Amendments of the Specification

Please replace the paragraph at page 6, lines 10-23, with the following amended paragraph:

The circuitry of this invention may further be programmable to support a higher data clock rate than the highest clock rate associated with either the reference clock signal or the operation of a phase locked loop (PLL) circuit within the CDR circuitry. A multiplexer can be programmed to select eight clock phases for a selected frequency from one of two PLLs whose frequency range contains the selected frequency. Alternatively, a single wide-range PLL can be used[[to]]. Two recovered clocks can be generated and used to lock and retime the serial input data. In the CDR receiver circuitry, the retimed data signals are deserialized. In the CDR transmitter circuitry, the retimed data signals are serialized.